

FIG. 1

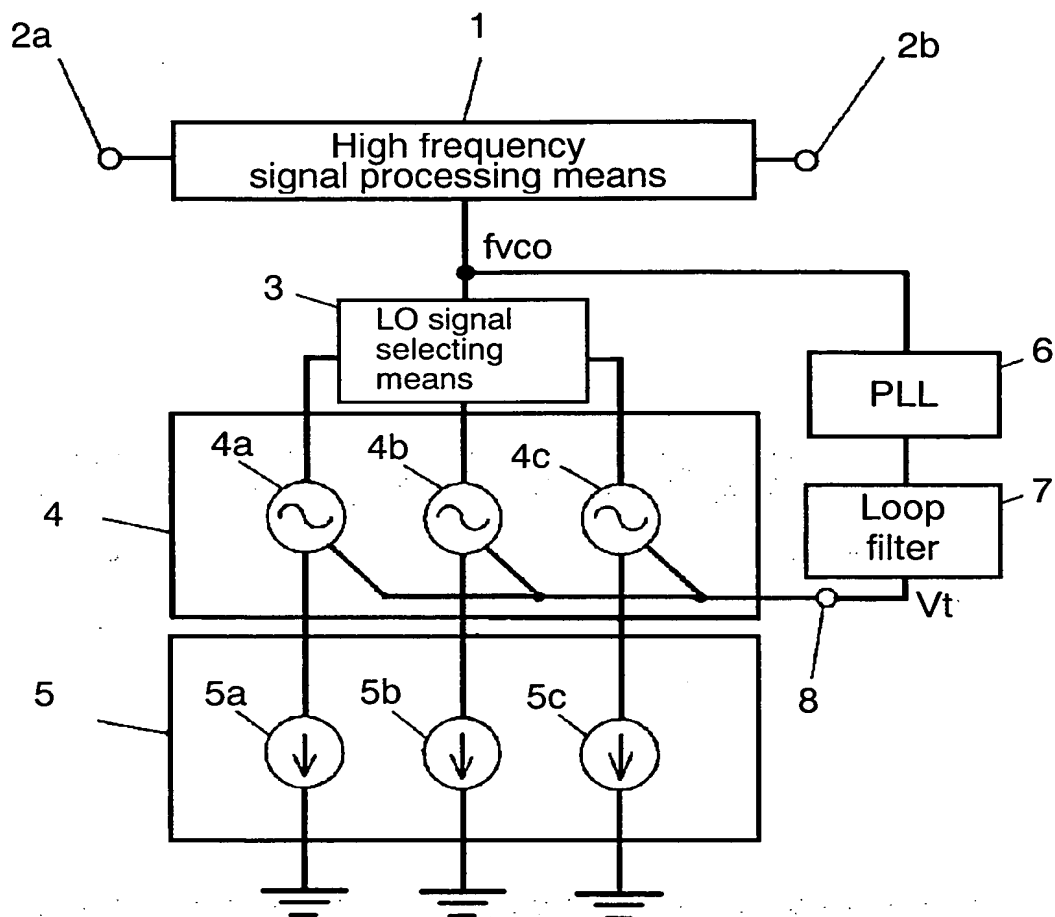
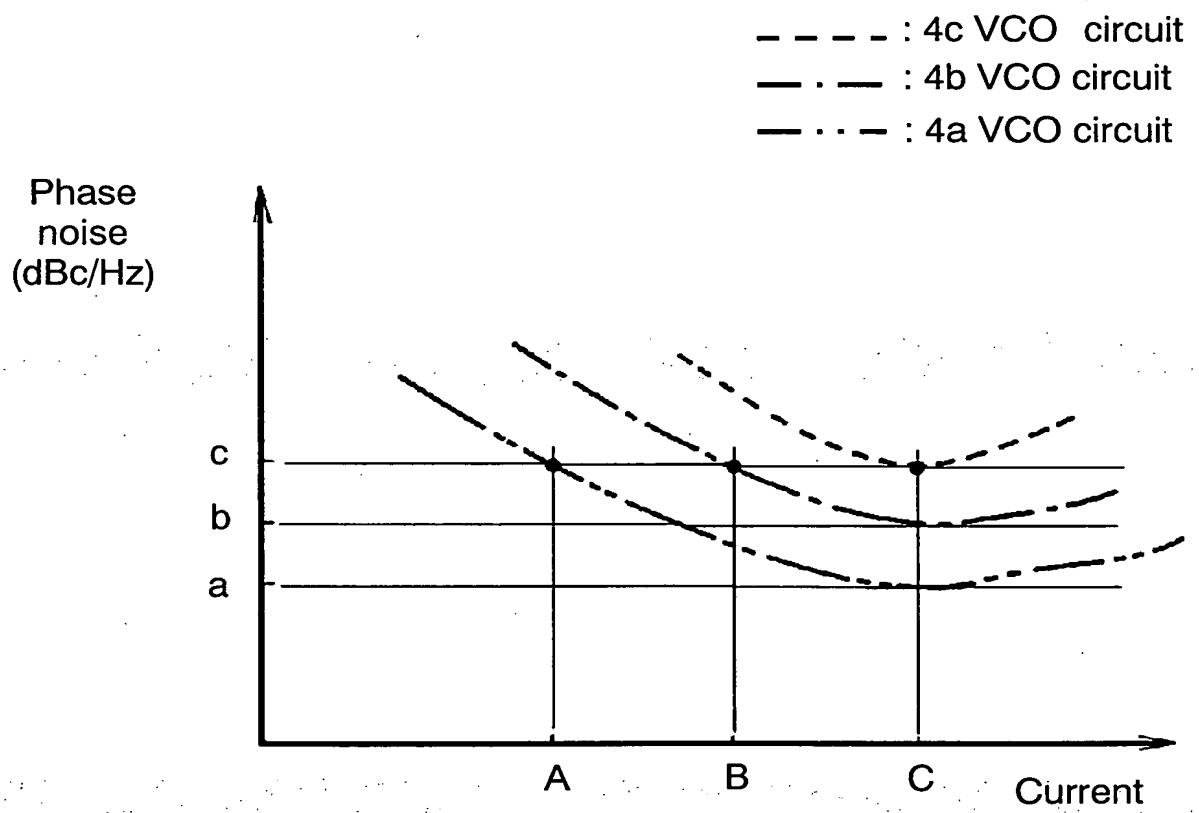


FIG. 2



3/20

FIG. 3

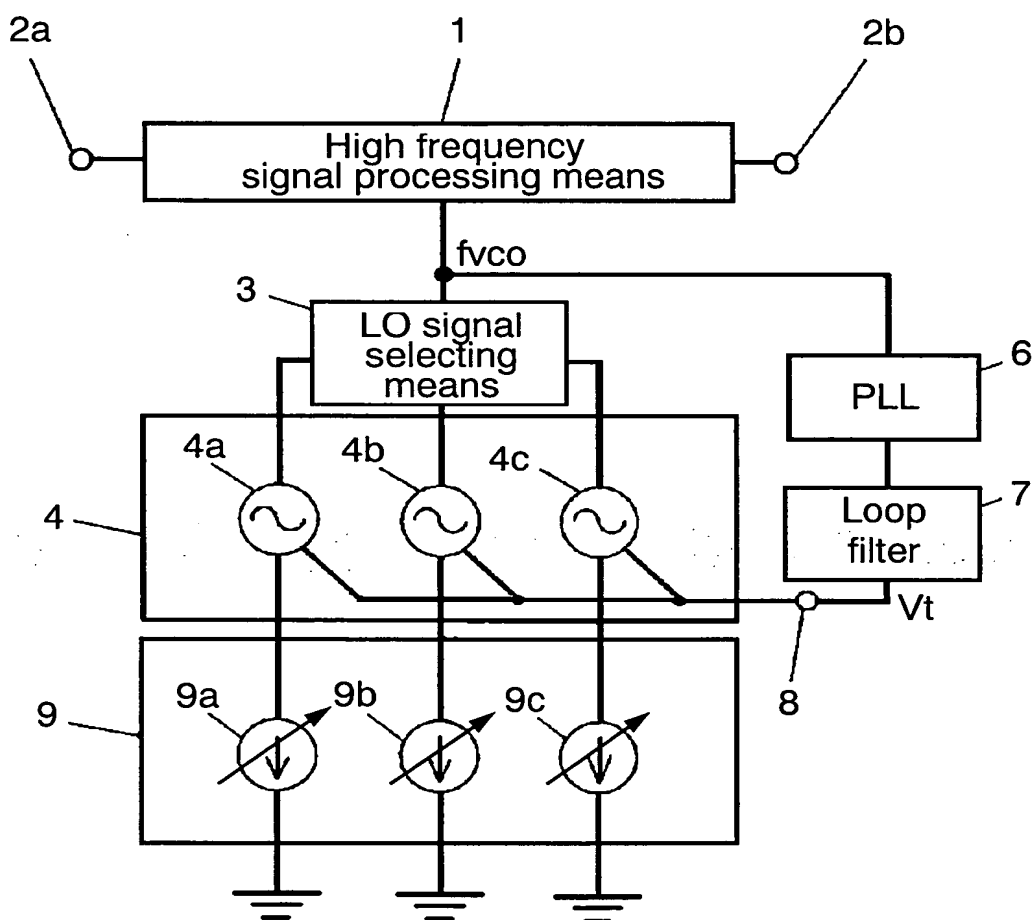
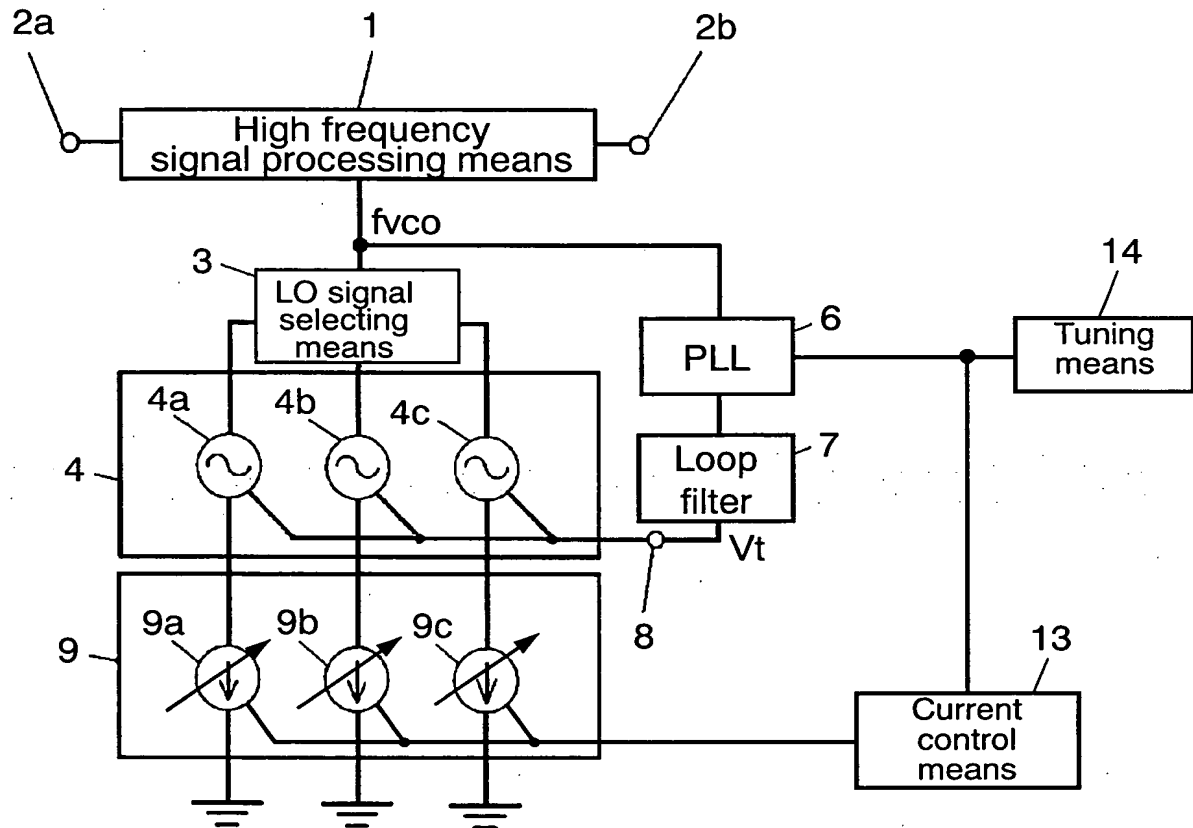
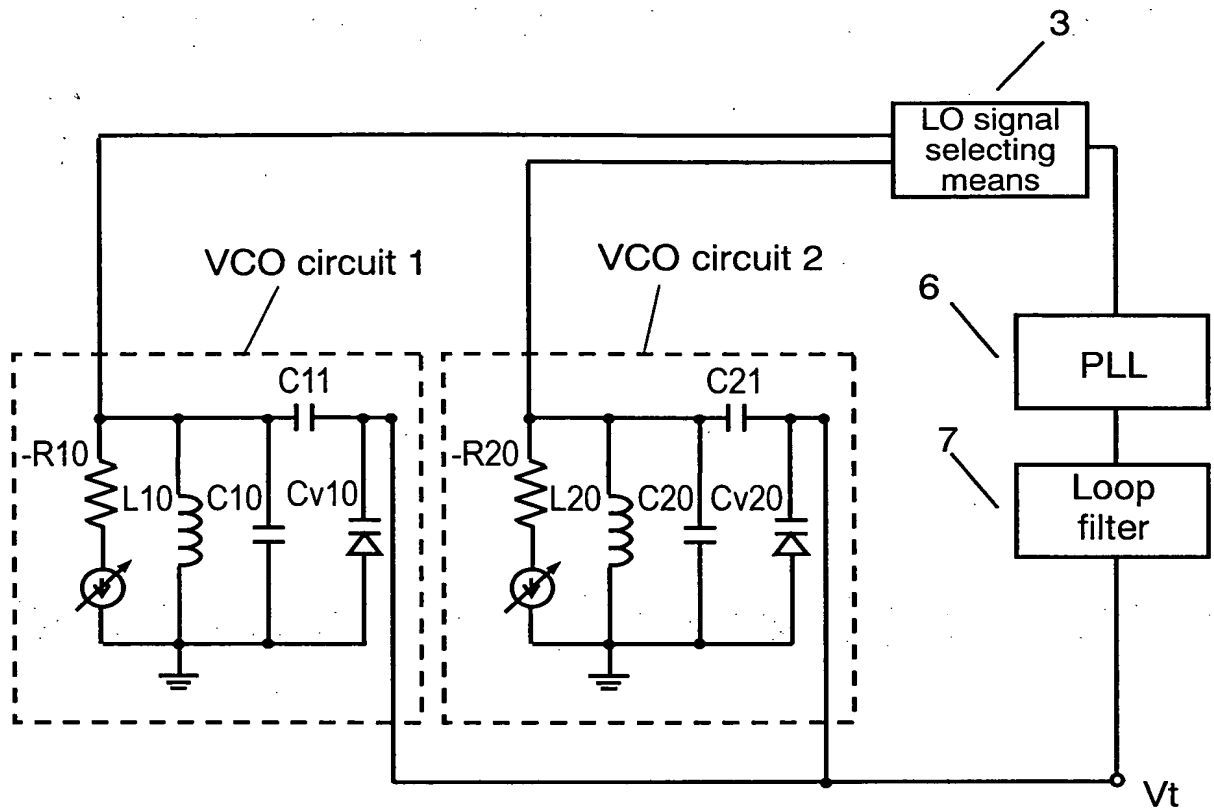


FIG. 4



5/20

FIG. 5



6/20

FIG. 6

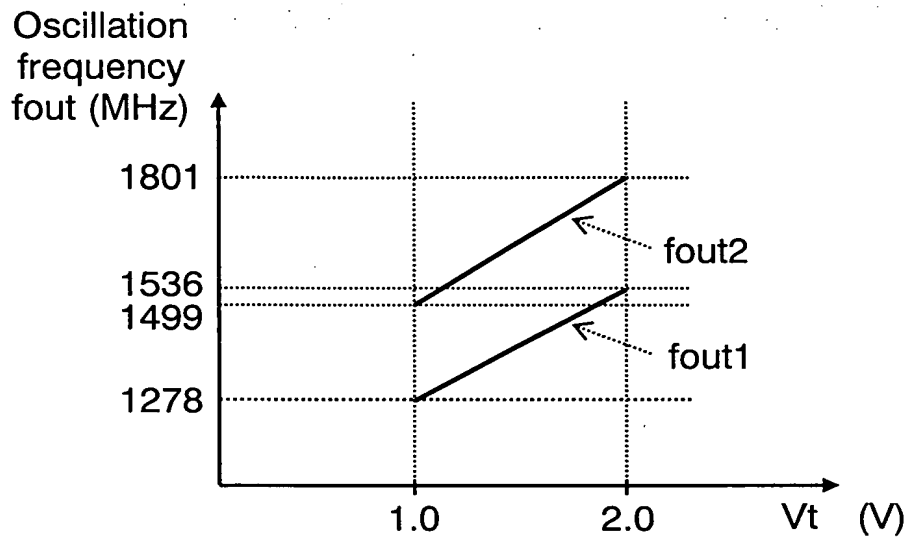
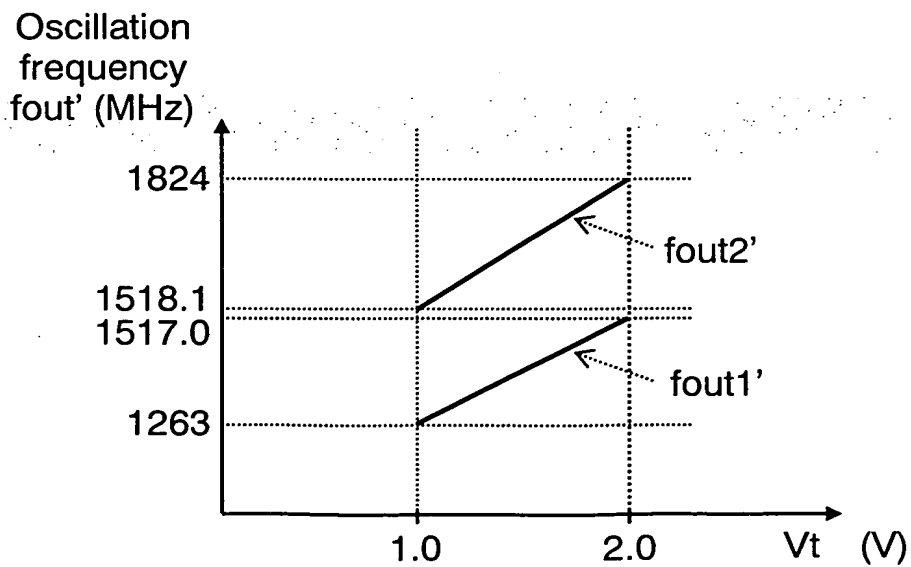


FIG. 7



7/20

FIG. 8

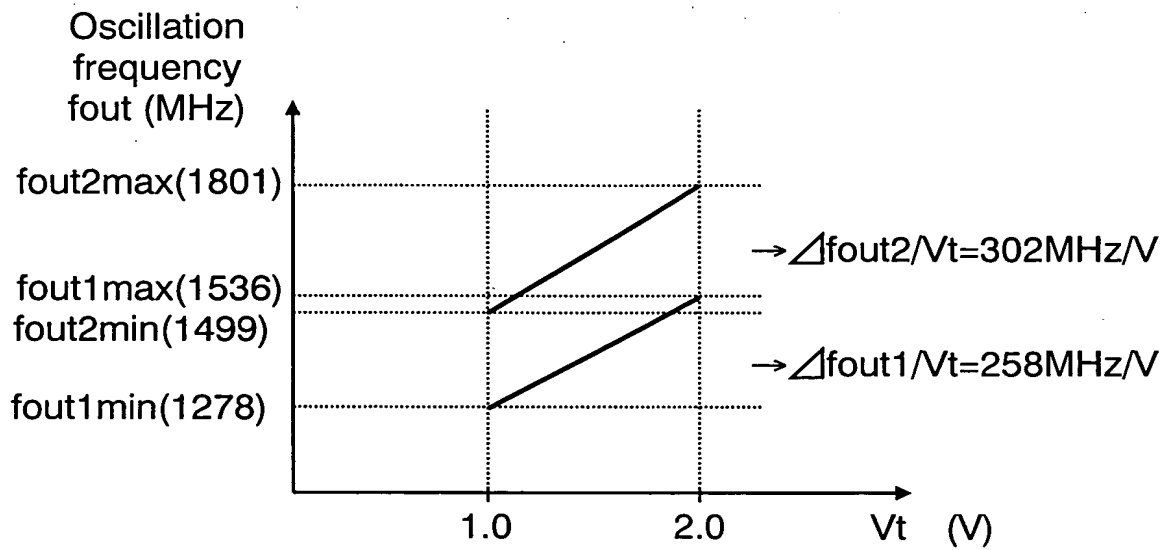


FIG. 9

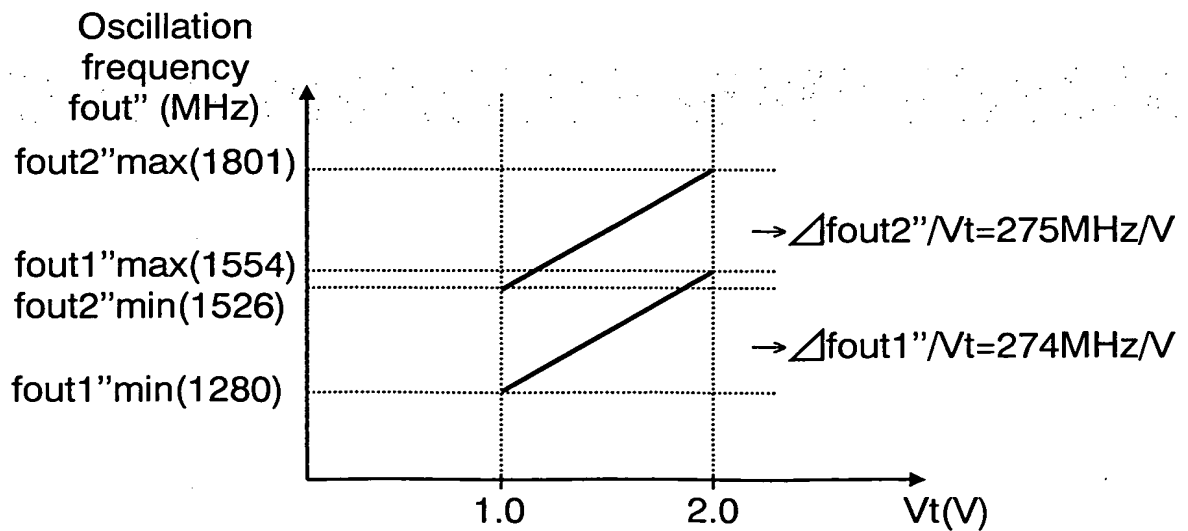
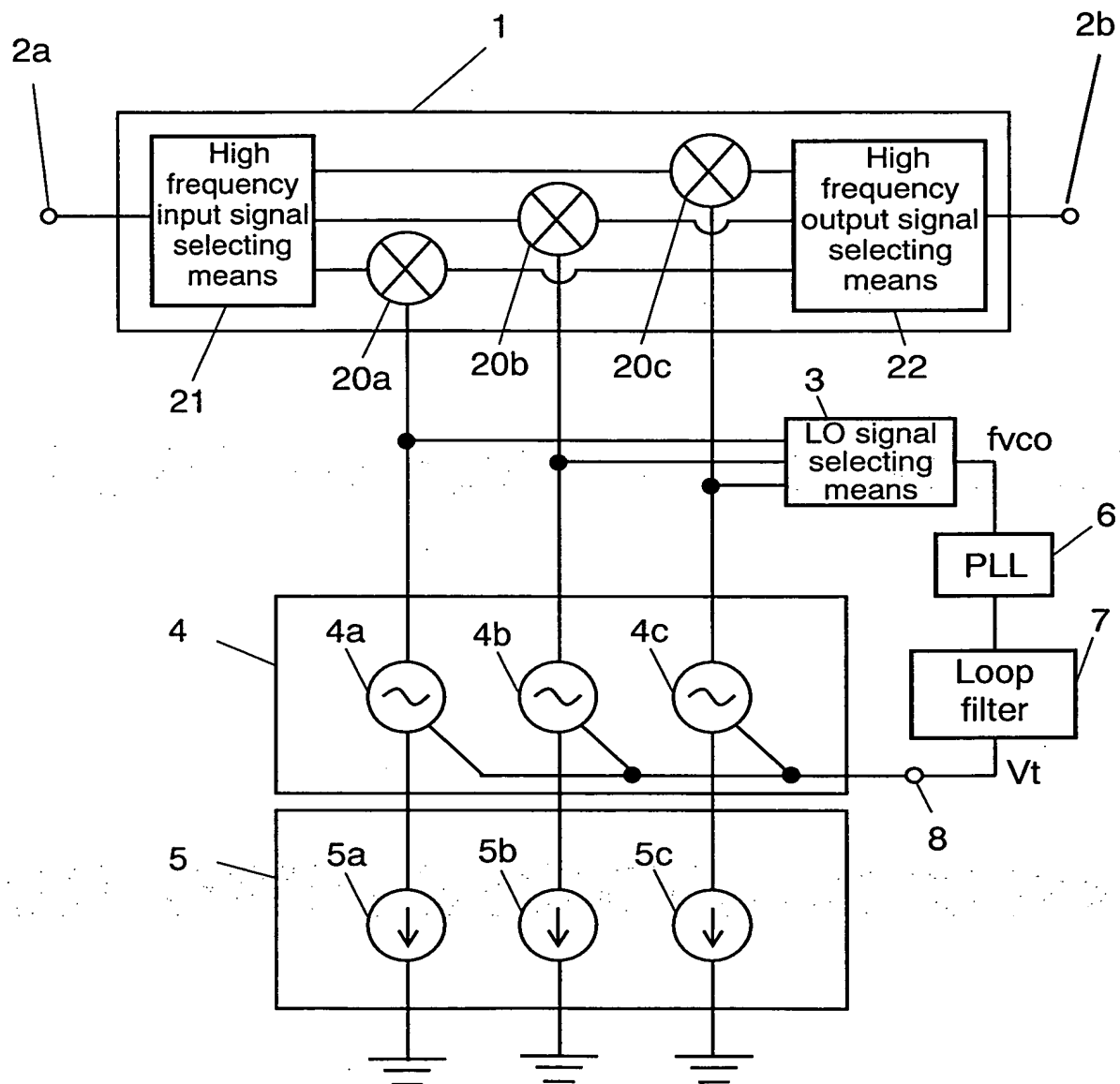


FIG. 10



9/20

FIG. 11

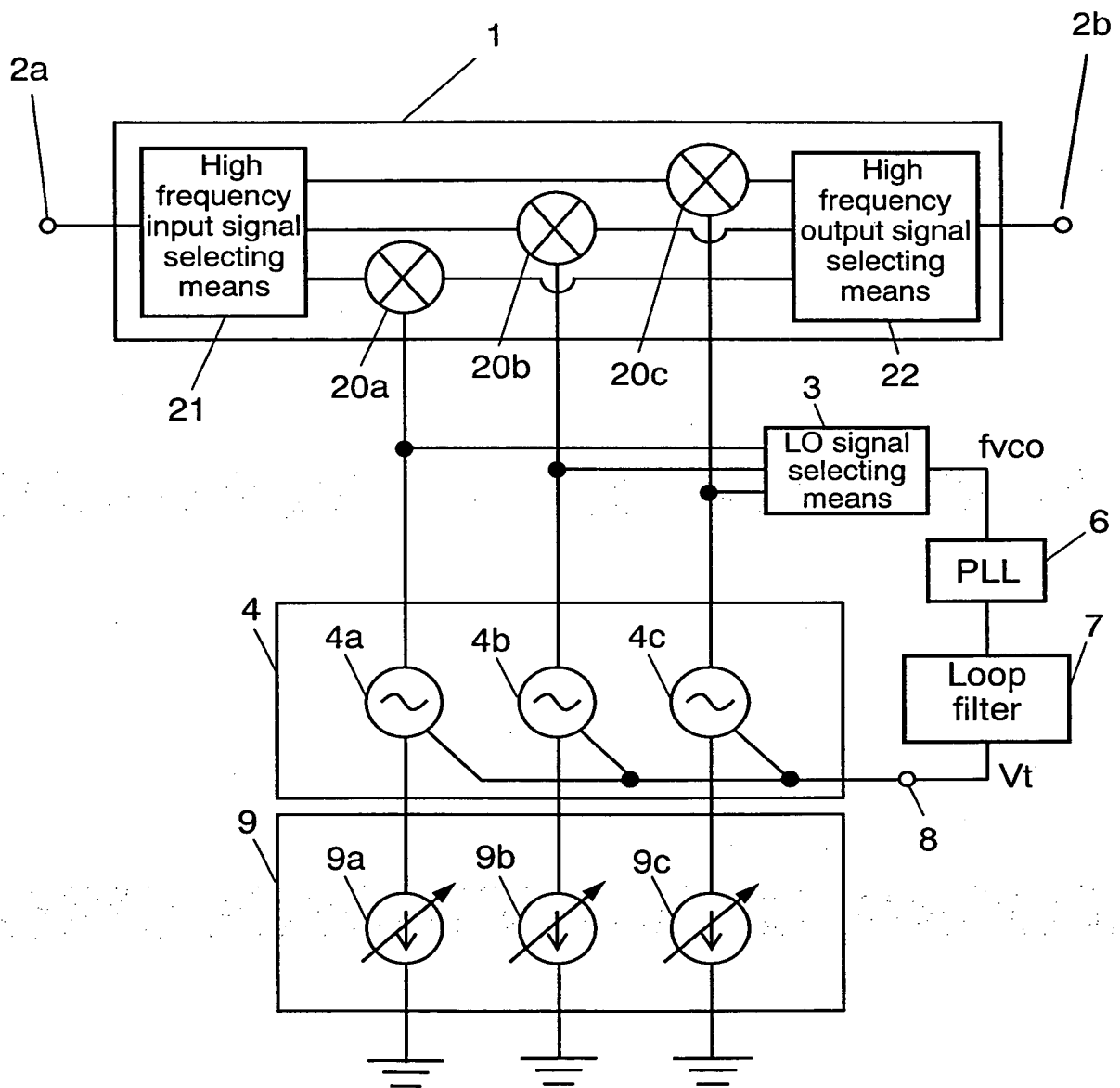
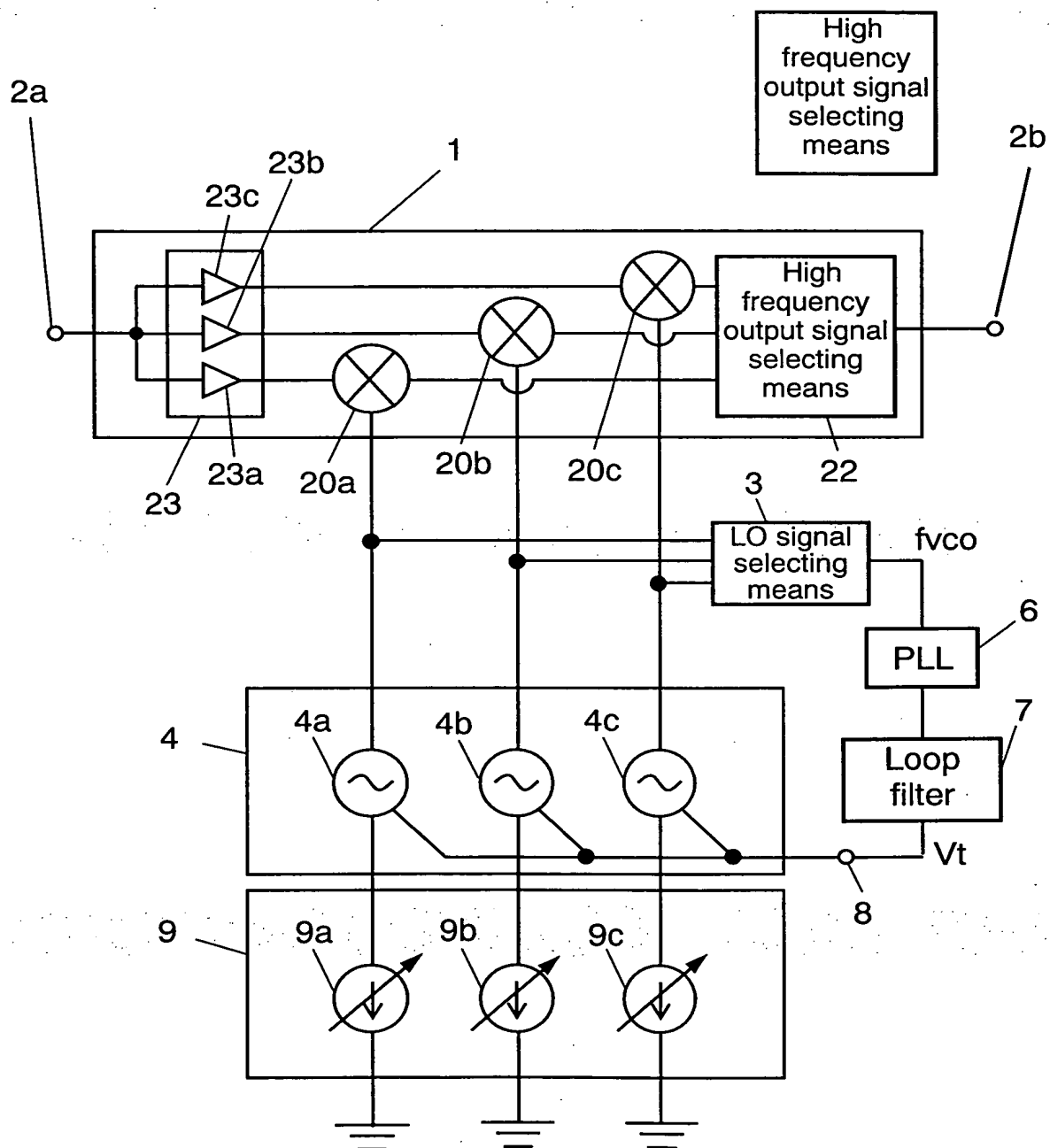
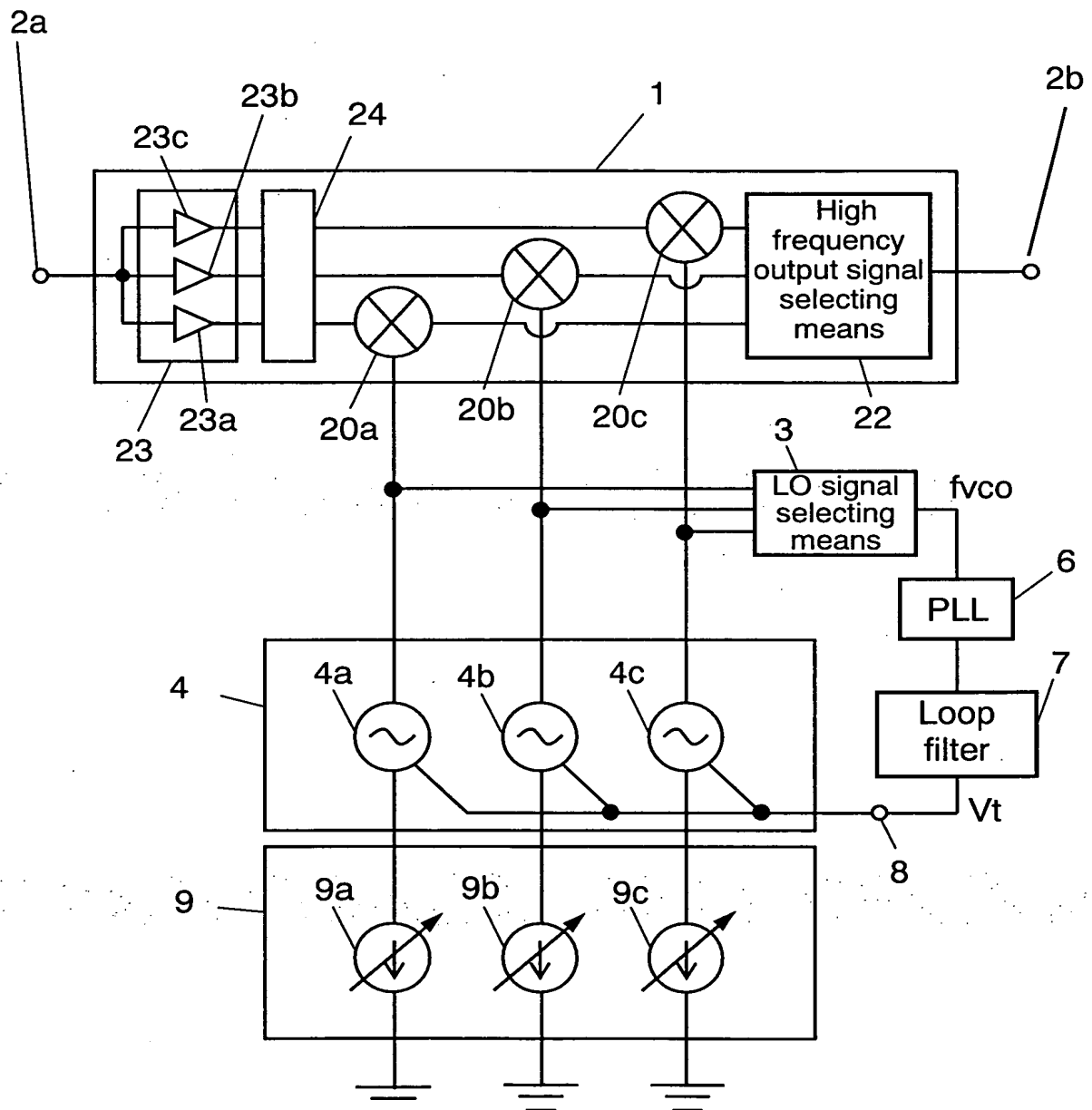


FIG. 12



11/20

FIG. 13



12/20

FIG. 14

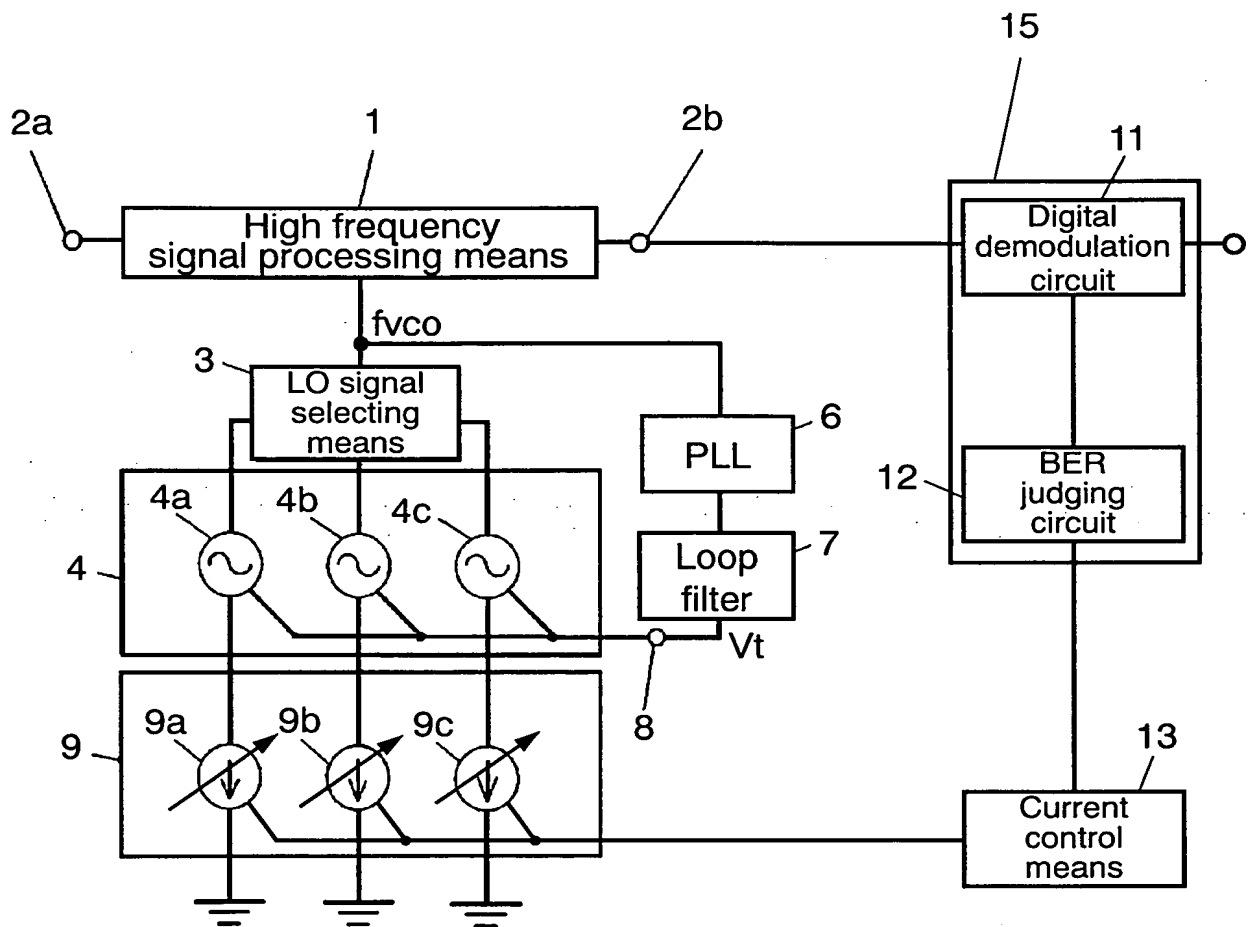
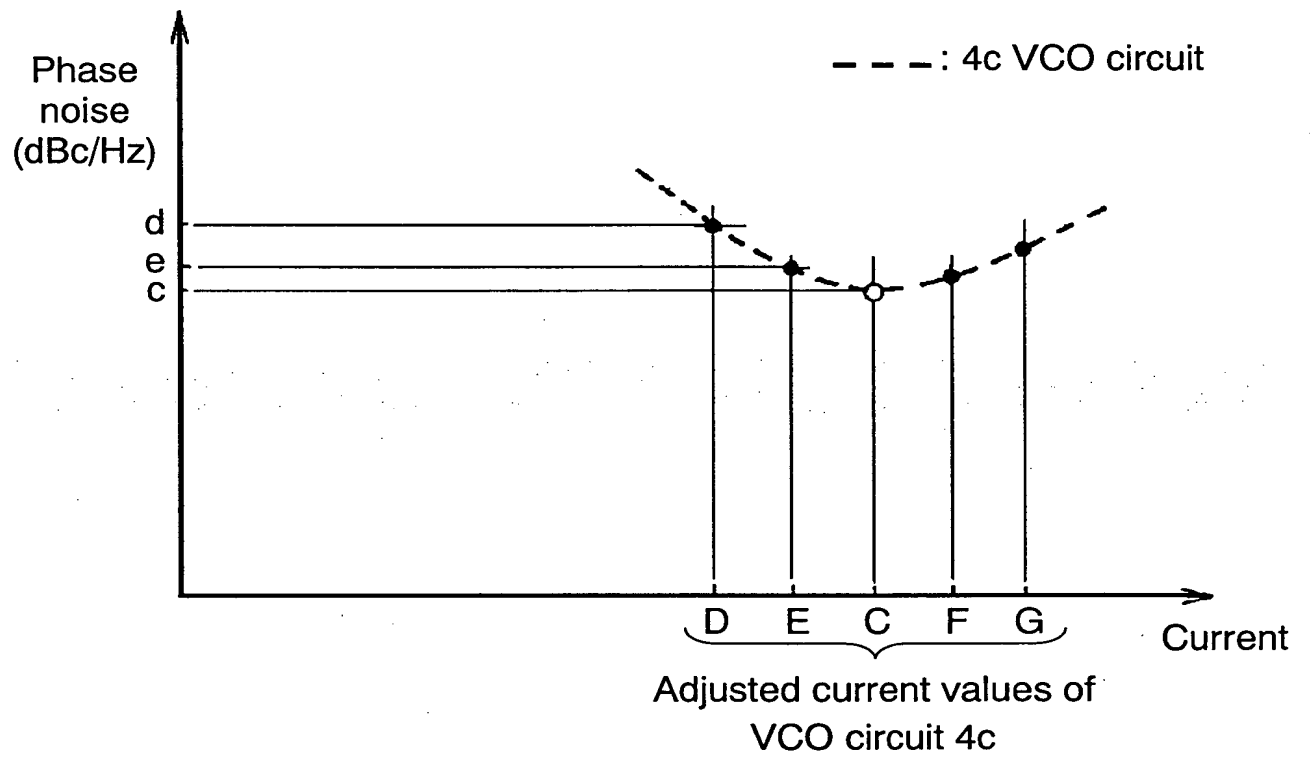


FIG. 15



14/20

FIG. 16

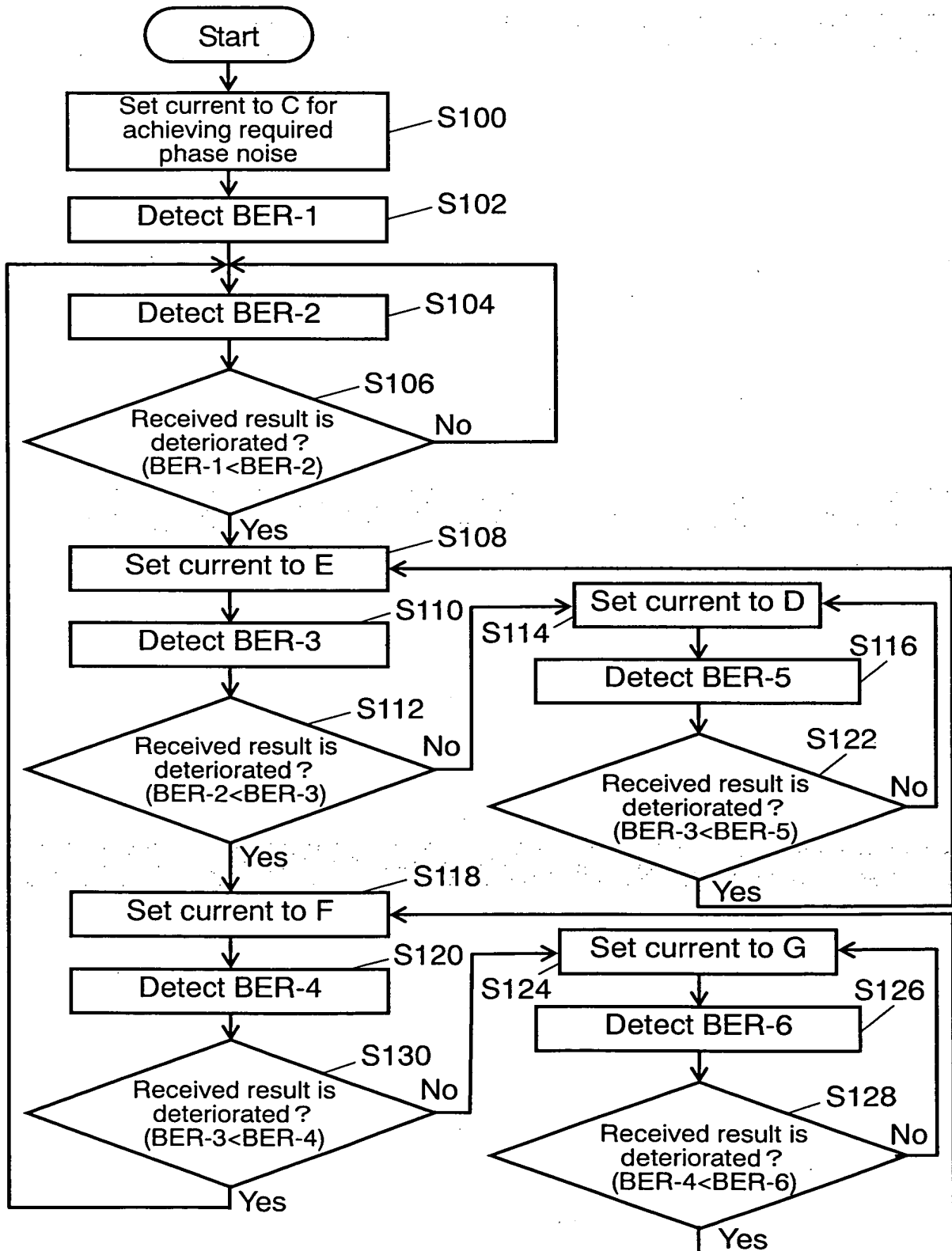


FIG. 17

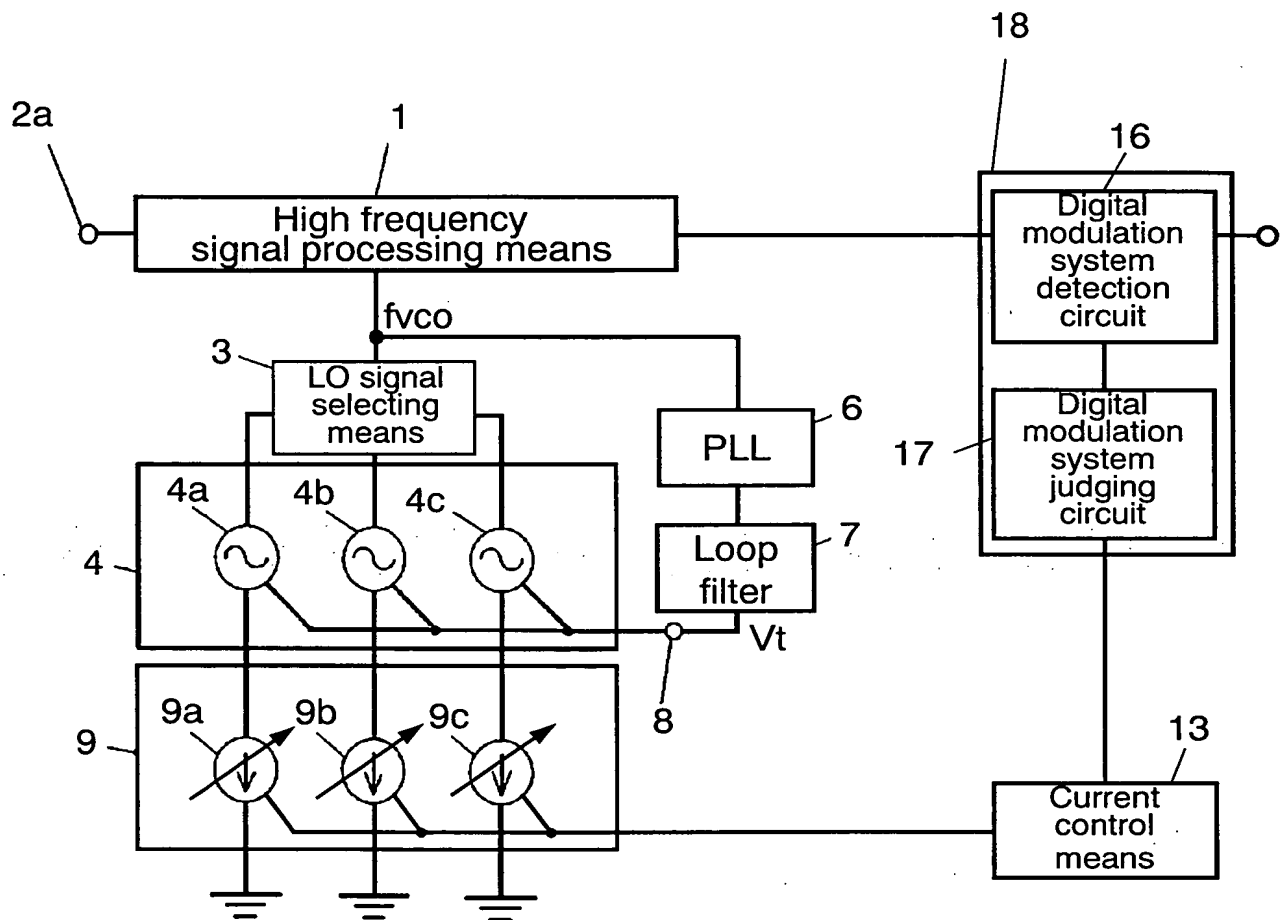
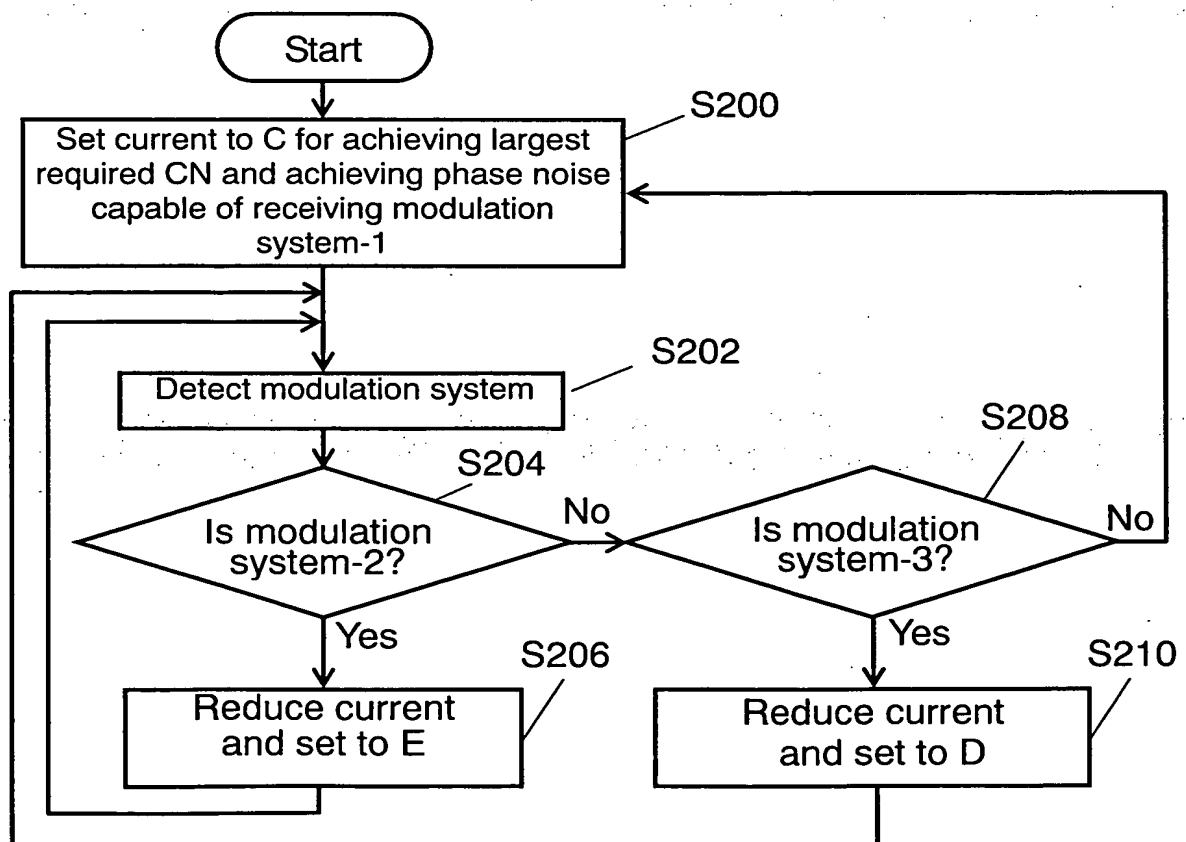


FIG. 18

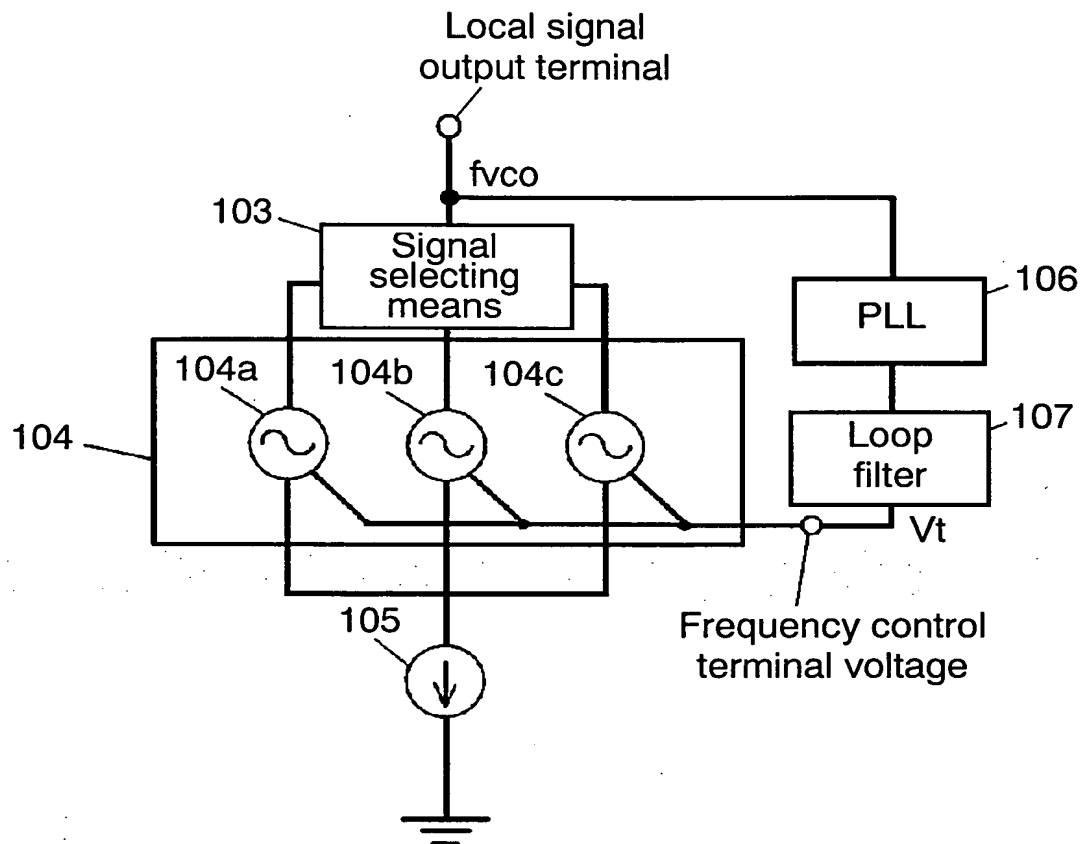
Digital modulation system (required CNR of receiver)	Modulation system (1) (required CNR=large)	Modulation system (2) (required CNR=middle)	Modulation system (3) (required CNR=small)
Phase noise and current amount of VCO	Phase noise=c	Phase noise=e	Phase noise=d
	Current amount=C	Current amount=E	Current amount=D

FIG. 19



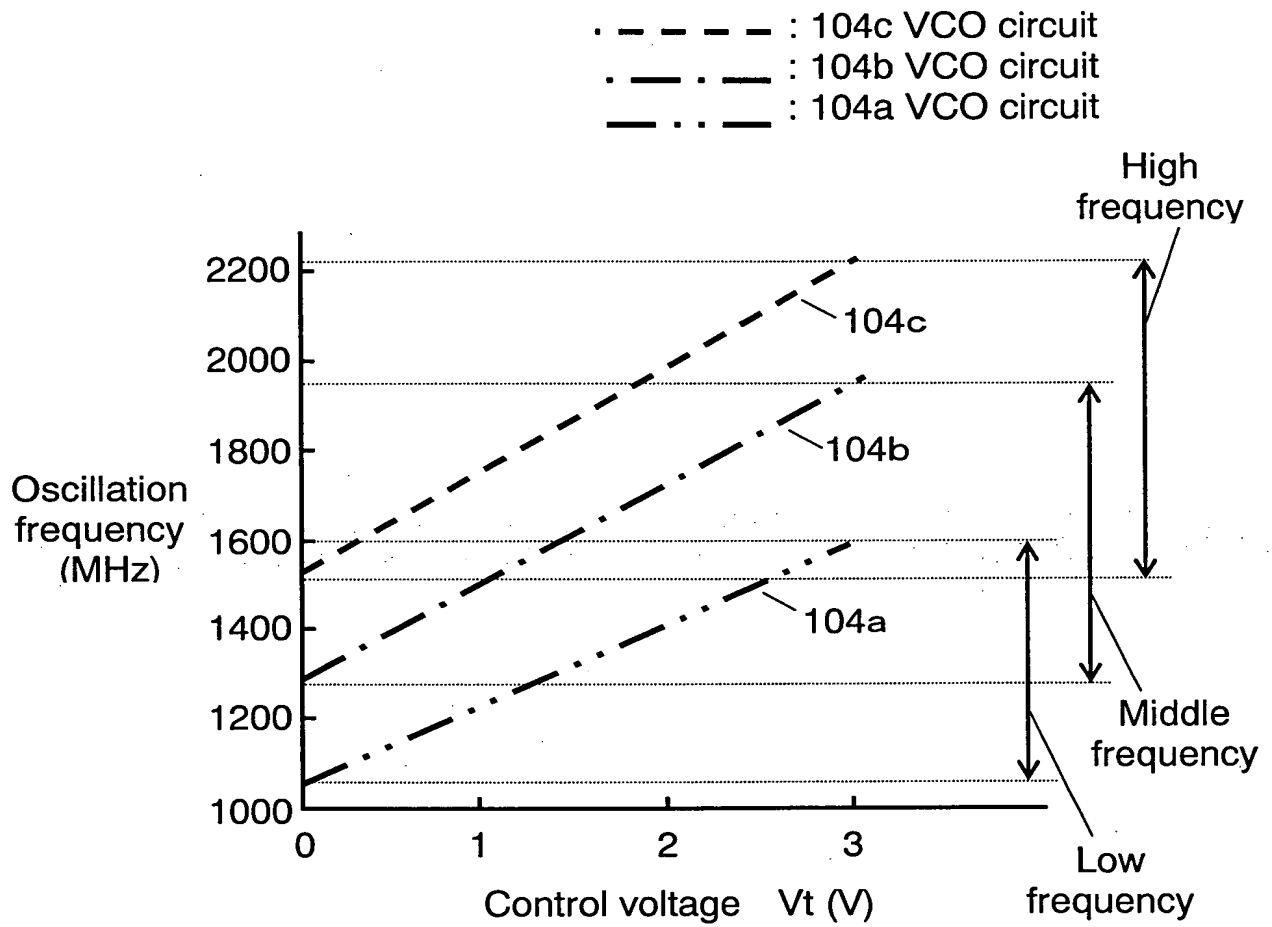
17/20

FIG. 20



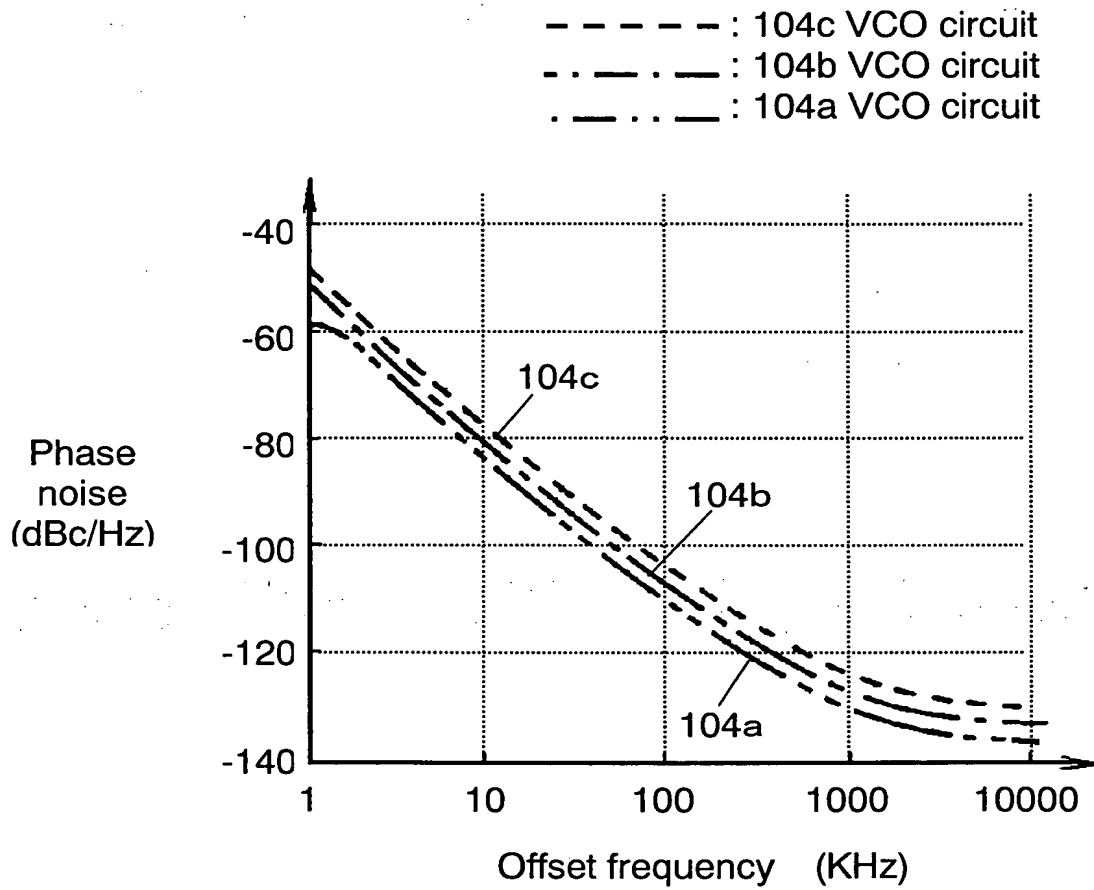
18/20

FIG. 21



19/20

FIG. 22



REFERENCE NUMERALS IN THE DRAWINGS

- 1 High frequency signal processing means
- 2a High frequency signal input terminal
- 2b High frequency signal output terminal
- 3 LO signal selecting means
- 4 VCO circuit group
- 4a, 4b, 4c VCO circuit
- 5, 9 Current source circuit group
- 5a, 5b, 5c Current source circuit
- 6: PLL
- 7 Loop filter
- 8 Frequency control voltage terminal
- 9a, 9b, 9c Variable current source circuit
- 11 Digital demodulation circuit
- 12 BER judging circuit
- 13 Current control means
- 14 Tuning means
- 15 Received characteristics judging means
- 16 Digital modulation system detection circuit
- 17 Digital modulation system judging circuit
- 18 Digital modulation system judging means
- 20a, 20b, 20c MIX circuit
- 21 High frequency input signal selecting means
- 22 High frequency output signal selecting means
- 23 Low phase noise amplifier group (LNA group)
- 23a, 23b, 23c Low phase noise amplifier (LNA)
- 24: BFP